IN THE CLAIMS

Please amend claims 1, 3, 4, 9, 10, 16 and 19 as set forth below.

1. (Currently Amended) A semiconductor device comprising:

A1

a first semiconductor chip having on one main surface thereof a control circuit, a first bonding pad, and a plurality of second bonding pads;

a second semiconductor chip having on one main surface thereof a memory circuit and a third bonding pad and disposed on the one main surface of the first semiconductor chip, the memory circuit being controlled in accordance with a control signal generated in the control circuit on the first semiconductor chip;

a first lead having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip;

a plurality of second leads each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip;

a first bonding wire for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the first lead;

a plurality of second bonding wires for connecting the plural second bonding pads on the first semiconductor chip with the inner lead portions of the plural second leads;

a third bonding wire for connecting the third bonding pad on the second semiconductor chip with the inner lead portion of the first lead; and

a resin seal member for sealing the first and second semiconductor chips, the first, second and third bonding wires, and the inner lead portions of the first and second leads,

wherein the control signal generated in the control circuit is outputted from the first bonding pad on the first semiconductor chip and is inputted to the third bonding pad on the second semiconductor chip through the first bonding wire, the first lead and the third bonding wire.

2. (Original) A semiconductor device according to claim 1, wherein the second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.

3. (Currently Amended) A semiconductor device according to claim 1, wherein another main surface of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip ~~in an opposed relation to~~ so as to be facing the one main surface of the first semiconductor chip.

4. (Currently Amended) A semiconductor device according to claim 1, wherein the first and third bonding wires are connected to ~~one and~~ the same surface of the first lead.

5. (Original) A semiconductor device comprising:

a first semiconductor chip having on one main surface thereof a processor unit adapted to operate in accordance with a program and a plurality of bonding pads;

a second semiconductor chip having on one main surface thereof a non-volatile memory unit into which are written serial data by operation of the first semiconductor chip and also having a plurality of bonding pads, the second semiconductor chip being disposed on one main surface of the first semiconductor chip;

a plurality of leads each having an inner lead portion and an outer lead portion integral with the inner lead

portion, the inner lead portion being disposed at a position around the first semiconductor chip; and

a resin seal member for sealing the first and second semiconductor chips and the inner lead portions of the plural leads,

wherein the plural bonding pads on the first and second semiconductor chips are electrically connected to the inner lead portions of the plural leads.

6. (Original) A semiconductor device according to claim 5,

wherein the first semiconductor chip is a chip for a microcomputer, and

wherein the second semiconductor chip is a chip for an EEPROM.

7. (Original) A semiconductor device according to claim 5,

wherein the plural bonding pads on the first semiconductor chip include a first bonding pad,

wherein the plural bonding pads on the second semiconductor chip include a second bonding pad,

wherein the first bonding pad is electrically connected to an inner lead portion of one of the plural leads through a first bonding wire,

wherein the second bonding pad is electrically connected to an inner lead portion of one of the plural leads through a second bonding wire, and

wherein the serial data are outputted from the first bonding pad and inputted to the second bonding pad through the first bonding wire, one of the plural leads, and the second bonding wire.

8. (Original) A semiconductor device according to claim 5, wherein the second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.

9. (Currently Amended) A semiconductor device according to claim 5, wherein another main surface of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip ~~in an opposed relation to~~ so as to be facing the one main surface of the first semiconductor chip.

10. (Currently Amended) A semiconductor device according to claim 6, wherein the first and second bonding wires are connected to ~~one and~~ the same surface of one of the plural leads.

11. (Original) A semiconductor device comprising:

a first semiconductor chip having on one main surface thereof a first bonding pad and a plurality of second bonding pads;

a second semiconductor chip having on one main surface thereof a plurality of third bonding pads interconnected electrically, the second semiconductor chip being disposed on the one main surface of the first semiconductor chip;

a first lead having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip;

a plurality of second leads each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip;

a first bonding wire for connecting the first bonding pad on the first semiconductor chip with the inner lead of the first lead;

a plurality of second bonding wires for connecting the plural second bonding pads on the first semiconductor chip with the inner lead portions of the plural second leads;

a third bonding wire for connecting one of the plural third bonding pads on the second semiconductor chip with the inner lead portion of the first lead; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portions of the first, second and third leads, and the first, second and third bonding wires.

12. (Original) A semiconductor device according to claim 11,

wherein the second semiconductor chip is formed in a quadrangular shape in plan, and

wherein the plural third bonding pads are arranged along at least one side of the second semiconductor chip.

13. (Original) A semiconductor device according to claim 11,

wherein the second semiconductor chip is formed in a quadrangular shape in plan, and

wherein the plural third bonding pads are arranged along at least two sides contiguous to each other of the second semiconductor chip.

14. (Original) A semiconductor device according to claim 11, wherein the first bonding pad and the plural third bonding pads are bonding pads for signal.

15. (Original) A semiconductor device according to claim 11, wherein the second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.

16. (Currently Amended) A semiconductor device according to claim 11, wherein another main surface of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip ~~in an opposed relation to~~ so as to be facing the one main surface of the first semiconductor chip.

17. (Original) A semiconductor device according to claim 11, wherein the first and third bonding wires are connected to one and same surface of the first lead.

18. (Original) A semiconductor device comprising:

a first semiconductor chip having on one main surface thereof a first bonding pad and a second bonding pad both disposed along one side of the one main surface;

a second semiconductor chip quadrangular in shape and having on one main surface thereof a third bonding pad and two fourth bonding pads interconnected electrically, the third and fourth bonding pads being disposed along one side of the one main surface of the second semiconductor chip, the third bonding pad being disposed between the fourth bonding pads, the second semiconductor chip being disposed on the one main surface of the first semiconductor chip in such a manner that the one side of the one main surface thereof is opposite to the one side of the one main surface of the first semiconductor chip;

a first lead and a second lead each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed outside the one side of the first semiconductor chip;

a first bonding wire for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the first lead;

a second bonding wire for connecting the second bonding pad on the first semiconductor chip with the inner lead portion of the second lead;

a third bonding wire for connecting the third bonding pad on the second semiconductor chip with the inner lead portion of the first lead;

a fourth bonding wire for connecting one of the two fourth bonding pads on the second semiconductor chip with the inner lead portion of the second lead; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portions of the first and second leads, and the first, second, third and fourth bonding wires.

19. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip which is quadrangular and which has a first bonding pad on one side of one main surface thereof;

a second semiconductor chip which is quadrangular and which has a second bonding pad on one side of one main surface thereof, the one side of the one main surface of the second semiconductor chip being disposed on the one main surface of the first semiconductor chip ~~in an opposed relation to~~ so as to be facing the one side of the one main surface of the first semiconductor chip;

a lead having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed outside the one side of the first semiconductor chip;

a first bonding wire connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the lead;

a second bonding wire for connecting the second bonding pad on the second semiconductor chip with the inner lead portion of the lead; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portion of the lead, and the first and second bonding wires,

wherein the second semiconductor chip is disposed on the one main surface of the first semiconductor chip in a state such that a central point of the second semiconductor

chip is displaced so as to be positioned on one side of the first semiconductor chip with respect to a central point of the first semiconductor chip.

20. (Original) A semiconductor device according to claim 19,

wherein the central point of the first semiconductor chip is a point of intersection of a first center line extending in the same direction as the one side of the first semiconductor chip and a second center line orthogonal to the first center line, and

wherein the central point of the second semiconductor chip is a point of intersection of a first center line extending in the same direction as the one side of the second semiconductor chip and a second center line orthogonal to the first center line.

21. (Original) A semiconductor device comprising:

a first semiconductor chip which is quadrangular in plan and which has a first bonding pad on a first side of one main surface thereof and a second bonding pad on a second side of the one main surface contiguous to the first side;

a second semiconductor chip which is quadrangular in plan and which has a third bonding pad on one side of one main surface thereof and a fourth bonding pad on a second side of the one main surface contiguous to the first side;

the second semiconductor chip being disposed on the one main surface of the first semiconductor chip in a state such that the first side of the one main surface thereof is opposed to the first side of the first semiconductor chip and the second side of the one main surface thereof is opposed to the second side of the first semiconductor chip;

a first lead having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed outside the first side of the first semiconductor chip;

a second lead having an inner lead portion and an outer lead potion integral with the inner lead portion, the inner lead portion being disposed outside the second side of the first semiconductor chip;

a first bonding wire for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the first lead;

a second bonding wire for connecting the first bonding pad on the second semiconductor chip with the inner lead of the first lead;

a third bonding wire for connecting the second bonding pad on the first semiconductor chip with the inner lead of the second lead;

a fourth bonding wire for connecting the second bonding pad on the second semiconductor chip with the inner lead of the second lead; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portions of the first and second leads, and the first to fourth bonding wires,

wherein the second semiconductor chip disposed on the one main surface of the first semiconductor chip in a state such that a central point thereof is displaced so as to be positioned on the first and second sides of the first semiconductor chip.

22. (Original) A semiconductor device according to claim 21,

wherein the central point of the first semiconductor chip is a point of intersection of a first center line extending in the same direction as the first side of the first

semiconductor chip and a second center line orthogonal to the first center line, and

wherein the central point of the second semiconductor chip is a point of intersection of a first center line extending in the same direction as the first side of the second semiconductor chip and a second center line orthogonal to the first center line.

23. (Original) A semiconductor device comprising:

a first semiconductor chip which is quadrangular and which has a first bonding pad on one side of one main surface thereof;

a second semiconductor chip which is quadrangular and which has a second bonding pad on one side of one main surface thereof, the second semiconductor chip being disposed on the one main surface of the first semiconductor chip;

a lead having an inner lead and an outer lead integral with the inner lead, the inner lead being disposed outside the one side of the first semiconductor chip;

a first bonding wire for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the lead;

a second bonding wire for connecting the second bonding pad on the second semiconductor chip with the inner lead portion of the lead; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portion of the lead, and the first and second bonding wires,

wherein the second semiconductor chip is disposed on the first semiconductor chip in a state such that one side of the second semiconductor chip is opposed to two sides contiguous to each other of the first semiconductor chip so as to shorten the length of the second bonding wire.

24. (Original) A semiconductor device comprising:

a first semiconductor chip having a first main surface and a second main surface opposed to each other, with a plurality of bonding pads being formed on the first main surface;

a second semiconductor chip having a first main surface and a second main surface opposed to each other, with a plurality of bonding pads being formed on the first main surface, the second semiconductor chip being disposed on the first semiconductor chip in a state such that the second main surface thereof is opposed to the first main surface of the

first semiconductor chip, the second semiconductor chip being smaller in plane size than the first semiconductor chip;

a plurality of leads each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip;

a plurality of bonding wires for connecting the plural bonding pads on the first and second semiconductor chips with the inner lead portions of the plural leads respectively; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portions of the plural leads, and the plural bonding wires, wherein the second semiconductor chip is smaller in thickness than the first semiconductor chip.

25. (Original) A semiconductor device according to claim 24, wherein the second semiconductor chip is bonded to the first main surface of the first semiconductor chip through an adhesive layer.

26. (Original) A semiconductor device according to claim 25, wherein the adhesive layer is formed by a bonding resin film.

27. (Original) A semiconductor device according to claim 25, wherein the distance from the first main surface of the first semiconductor chip to the second main surface of the second semiconductor chip is smaller than the thickness of the first semiconductor chip.

28. (Original) A semiconductor device comprising:

a first semiconductor chip having a first main surface and a second main surface opposed to each other, with a plurality of bonding pads being formed on the first main surface;

a second semiconductor chip having a first main surface and a second main surface opposed to each other, with a plurality of bonding pads being formed on the first main surface, the second semiconductor chip being disposed on the first semiconductor chip in a state such that the second main surface thereof is opposed to the first main surface of the first semiconductor chip, the second semiconductor chip being smaller in plane size than the first semiconductor chip;

a plurality of leads each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip;

a plurality of bonding wires for connecting the plural bonding pads on the first and second semiconductor chips with the inner lead portions of the plural leads respectively; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portions of plural leads, and the plural bonding wires,

wherein the bonding pads on the second semiconductor chip are larger in plane size than the bonding pads on the first semiconductor chip.

29. (Original) A semiconductor device comprising:

a first semiconductor chip having a first main surface and a second main surface opposed to each other, with a plurality of quadrangular bonding pads being formed on the first main surface;

a second semiconductor chip having a first main surface and a second main surface opposed to each other, with a plurality of quadrangular bonding pads being formed on the

first main surface, the second semiconductor chip being disposed on the first semiconductor chip in a state such that the second main surface thereof is opposed to the first main surface of the first semiconductor chip, the second semiconductor chip being smaller in plane size than the first semiconductor chip;

a plurality of leads each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip;

a plurality of first bonding wires for connecting the plural bonding pads on the first semiconductor chip with the inner lead portions of the plural leads respectively;

a plurality of second bonding wires for connecting the plural bonding pads on the second semiconductor chip with the inner lead portions of the plural leads respectively; and

a resin seal member for sealing the first and second semiconductor chips, the inner lead portions of the plural leads, and the first and second bonding wires,

wherein the bonding pads on the second semiconductor chip are each formed in a rectangular shape wherein a side located in an extending direction of the bonding wires is longer than a side opposed to the leads.

30. (Original) A semiconductor device according to claim 29, wherein the bonding pads on the second semiconductor chip are larger in plane size than the bonding pads on the first semiconductor chip.

31. (Original) A semiconductor device according to claim 29,

wherein the second bonding wires each have a first portion extending in a direction perpendicular to the first main surface of the second semiconductor chip and a second portion extending along the first main surface of the second semiconductor chip, and

wherein the first portion is positioned above the inner lead portions.